| PCN Number: | 20181005000.0 | PCN Date: | October 08, 2018 |
|---|---|---|---|
| Title: | Datasheet for DS90UB933-Q1, DS90UB913A-Q1 | | |
| Customer Contact: | PCN Manager | Dept: | Quality Services |

**Change Type:**

| | | | | | |
|---|---|---|---|---|---|
| ☐ | Assembly Site | ☐ | Design | ☐ | Wafer Bump Site |
| ☐ | Assembly Process | ☒ | Data Sheet | ☐ | Wafer Bump Material |
| ☐ | Assembly Materials | ☐ | Part number change | ☐ | Wafer Bump Process |
| ☐ | Mechanical Specification | ☐ | Test Site | ☐ | Wafer Fab Site |
| ☐ | Packing/Shipping/Labeling | ☐ | Test Process | ☐ | Wafer Fab Materials |
| | | | | ☐ | Wafer Fab Process |

## Notification Details

**Description of Change:**

Texas Instruments Incorporated is announcing an information only notification.
The product datasheet(s) is being updated as summarized below.
The following change history provides further details.

TEXAS INSTRUMENTS

**DS90UB933-Q1**

SNLS546B – AUGUST 2016 – REVISED SEPTEMBER 2018

**Changes from Revision A (December 2016) to Revision B** **Page**

- Added recommendation to ensure GPO2 is low when PDB goes high ..... 4
- Added external clock input frequency range ..... 6
- Added strap pin input current specification for MODE and IDX pins ..... 6
- Updated $T_{JIT1}$ PCLK input jitter in the external oscillator mode ..... 9
- Added that 0.45UI $T_{JIT2}$ maximum is when used with DS90UB934-Q1 and added new foot note ..... 9
- Added clarification on MODE pin description in PCLK from imager mode ..... 20
- Updated the MODE setting values to ratio from voltage ..... 21
- Updated IDX setting values to ratio from voltage ..... 26
- Added register "TYPE" column per legend ..... 28
- Added type and default value to the reserved register bits that were missing this information ..... 28
- Added that register 0x00[7:1] does not auto update IDX strapped address ..... 28
- Added description for 0x05 bits 1 and 0 (TX_MODE_12b and TX_MODE_10b) ..... 30
- Added reference to Power over Coax Application report ..... 35
- Clarified description on PDB pin usage during power up ..... 35
- Added paragraph to explain setting registers if GPO2 state is not determined when PDB goes high ..... 35
- Added GPO2 to suggested power-up sequencing diagram ..... 35
- Added timing constraint for PDB to GPO2 delay ..... 36
- Revised coax connection diagram to include pulldown resistor for GPO2 ..... 37
- Revised STP connection diagram to include pulldown resistor for GPO2 ..... 39

TEXAS INSTRUMENTS

**DS90UB913A-Q1**

SNLS443E – MAY 2013 – REVISED SEPTEMBER 2018

| Changes from Revision D (October 2016) to Revision E | Page |
|---|---|
| • Added recommendation to ensure GPO2 is low when PDB goes high | 6 |
| • Added Power Over Coax supply noise to the recommended operating conditions table | 8 |
| • Clarified PCLK clock frequency range and added external clock input frequency range | 8 |
| • Added strap pin input current specification for MODE and IDX pins | 9 |
| • Updated $T_{JIT1}$ PCLK input jitter in the external oscillator mode | 11 |
| • Added clarification on MODE pin description in PCLK from imager mode | 22 |
| • Updated pullup and pulldown resistor to $R_1$ and $R_2$ in MODE pin configuration diagram | 22 |
| • Updated the MODE setting values to ratio | 23 |
| • Updated pullup and pulldown resistor for IDX to $R_3$ and $R_4$ in the diagram | 28 |
| • Updated IDX setting values to ratio | 28 |
| • Updated register "TYPE" column per legend | 30 |
| • Added type and default value to the reserved register bits that were missing this information | 30 |
| • Added that register 0x00[7:1] does not auto update IDX strapped address | 30 |
| • Added description for 0x05 bits 1 and 0 (TX_MODE_12b and TX_MODE_10b) | 32 |
| • Clarified description on PDB pin usage during power up | 37 |
| • Added paragraph to explain setting registers if GPO2 state is not determined when PDB goes high | 37 |
| • Added GPO2 to suggested power-up sequencing diagram | 37 |
| • Added timing constraint for PDB to GPO2 delay | 38 |
| • Revised coax connection diagram to include pulldown resistor for GPO2 | 40 |
| • Revised STP connection diagram to include pulldown resistor for GPO2 | 42 |

The datasheet number will be changing.

| Device Family | Change From: | Change To: |
|---|---|---|
| DS90UB933-Q1 | SNLS546A | SNLS546B |
| DS90UB913A-Q1 | SNLS443D | SNLS443E |

These changes may be reviewed at the datasheet links provided.

http://www.ti.com/product/DS90UB933-Q1

http://www.ti.com/product/DS90UB913A-Q1

**Reason for Change:**

To accurately reflect device characteristics.

**Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):**

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

**Changes to product identification resulting from this PCN:**

None.

**Product Affected:**

| | | | |
|---|---|---|---|
| DS90UB933TRTVRQ1 | DS90UB933TRTVTQ1 | DS90UB913ATRTVJQ1 | DS90UB913ATRTVRQ1 |
| DS90UB913ATRTVTQ1 | | | |

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

| Location | E-Mail |
|---|---|
| USA | PCNAmericasContact@list.ti.com |
| Europe | PCNEuropeContact@list.ti.com |
| Asia Pacific | PCNAsiaContact@list.ti.com |
| Japan | PCNJapanContact@list.ti.com |